LISTING OF THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Previously Presented) A flip chip semiconductor device comprising a silicon wafer having parallel first and second major surfaces; at least one P region and at least one N region in said wafer which meet at a PN junction within said silicon wafer; first and second coplanar, laterally spaced and metallized layers formed on said first major surface and insulated form one another and connected to said P region and said N region respectively; a bottom metallized layer extending across said second major surface; and

a third metallized layer atop said first major surface which is coplanar with and laterally spaced from said first and second metallized layers; said first, second and third metallized layers comprising source, drain and gate electrodes respectively of a MOSgated device.

Claim 2. (Canceled)

3 (Original) The device of claim 1 which further includes at least one contact bump connected to each of said metallized layers.

4 (Previously Presented) The device of claim 1 which further includes at least one contact bump connected to each of said metallized layers.

5. (Original) The device of claim 1 wherein said bottom metallized layer is substantially thicker than all of said first and second metallized layers.

6. (Previously Presented) The device of claim 1 wherein said bottom metallized layer is substantially thicker than all of said first and second metallized layers.

7. (Previously Presented) The device of claim 1 wherein said bottom metallized layer is substantially thicker than all of said first and second metallized layers.

8. (Original) The device of claim 4 wherein said bottom metallized layer is substantially thicker than all of said first and second metallized layers.

9. (Previously Presented) The device of claim 1 wherein a plurality of contact bumps are connected to each of said first and second metallized layers; said plurality of contact bumps connected to said first metallized layer being aligned along a first straight row; said plurality of contact bumps connected to said second metallized layer being aligned along a second straight row.

10. (Original) The device of claim 9 wherein said first and second rows are parallel to one another.

Claim 11. (Canceled)

12. (Previously Presented) A flip chip semiconductor device comprising a silicon wafer having first and second parallel major surfaces; at least one P region and at least one N region in said wafer which meet at a PN junction within said silicon wafer; first and second coplanar, laterally spaced metallized layers formed on said first major surface and insulated form one another and connected to said P region and said N region respectively; a third metallized layer atop said first major surface which is coplanar with and laterally spaced from said first and second metallized layers; said first, second and third metallizing layers comprising source, drain and gate electrodes respectively of a MOSgated device; and a plurality of contact bumps connected to each of said first and second metallized layers; said plurality of contact bumps connected to said first metallizing layer being aligned along a first straight row; said plurality of contact bumps connected to said second metallizing layer being aligned along a second straight row.

Claim 13. (Canceled)

14. (Previously Presented) The device of claim 12 further comprising a bottom metallized layer extending across said second major surface.

15. (Original) The device of claim 12 wherein said bottom metallized layer is substantially thicker than all of said first and second metallized layers.

16. (Original) The device of claim 12 wherein said first and second rows are parallel to one another.

17. (Original) The device of claim 12 wherein said silicon wafer is a rectangular wafer having an area defined by a given length and a given width, said length being greater than said width; said first and second rows of bumps being parallel to one another and being symmetric about a diagonal line across said wafer.

18. (Original) The device of claim 17 which includes a third metallized layer atop said first major surface which is coplanar with and laterally spaced from said first and second metallized layers; said first, second and third metallized layers comprising source, drain and gate electrodes respectively of a MOSgated device.

19. (Original) The device of claim 14 wherein said silicon wafer is a rectangular wafer having an area defined by a given length and a given width, said length being greater than said width; said first and second rows of bumps being parallel to one another and being symmetric about a diagonal line across said wafer.

20. (Original) The device of claim 12 which further includes a bottom metallized layer extending across said second major surface.

Claims 21-29 (Canceled)